Amendments to the Claims

This listing will replace all prior versions, and listing, of claims in the application.

1. (currently amended) A method of forming a dual damascene structure for copper dual damascene processes, comprising ~~the steps of~~:

providing a substrate, said substrate having been provided with semiconductor devices structures ~~in or on the surface thereof~~, at least one point of electrical contact having been provided in ~~the surface of~~ said substrate, a layer of Inter Metal Dielectric (IMD) having been deposited over ~~the surface of~~ said substrate, at least one opening having been created through said layer of IMD, said at least one opening being aligned with said at least one point of electrical contact ~~having been provided in the surface of said substrate~~;

depositing a layer of first material over ~~the surface of~~ said layer of IMD, filling said at least one opening ~~created through said layer of IMD~~;

removing said layer of first material from ~~the surface of~~ said layer of IMD, thereby partially removing

said first material from said at least one opening ~~created through said layer of IMD~~, creating at least one partial opening through said layer of IMD, said at least one partial opening having a first and a second cross section;

baking said substrate for a period of time by applying an elevated temperature in a gaseous environment and under a pressure to said substrate;

depositing a layer of second material over ~~the surface of~~ said layer of IMD, thereby filling said second cross section of said at least one partial opening ~~created through said layer of IMD~~; and

patterning and etching said layer of second material, creating an opening through said layer of second material that aligns with said at least one partial opening created through said layer of IMD, removing said layer of second material from said second cross section of said at least one partial opening created through said layer of IMD.

2. (previously presented) The method of claim 1, said first material comprising I-line photoresist.

3. (previously presented) The method of claim 1, said second material comprising DUV photoresist.

4. (original) The method of claim 1, wherein said baking said substrate comprises baking said substrate on a hot plate.

5. (original) The method of claim 1, wherein said baking said substrate comprises baking said substrate inside a high-temperature furnace.

6. (original) The method of claim 1, wherein said applying an elevated temperature comprises applying a temperature between about 200 and 400 degrees C.

7. (original) The method of claim 1, wherein said pressure comprises a low pressure environment of between about 40 and 60 pa.

8. (original) The method of claim 1, wherein said pressure comprises an atmospheric pressure.

9. (original) The method of claim 1, wherein said gaseous environment may or may not contain an inert gas.

10. (original) The method of claim 1, wherein said gaseous environment may or may not contain an annealing agent that is typically applied for an anneal environment in which a metal is present.

11. (original) The method of claim 10, wherein said annealing agent is selected from the group consisting of H_2 and N_2 and NH_3.

12. (original) The method of claim 1, wherein said period of time is between about 1 and 30 minutes.

13. (currently amended) The method of claim 1, with additional steps being performed after said patterning and etching said second layer of material, said additional steps comprising:

depositing a layer of copper over ~~the surface of~~ said second layer of material, thereby filling said opening created through said second layer of material that aligns with said at least one partial opening created through said layer of IMD, thereby further filling said second cross section of said at least one partial opening created through said layer of IMD; and

removing said deposited layer of copper from ~~the surface of~~ said layer of second material.

14. (currently amended) The method of claim 13, said step of removing said deposited layer of copper from ~~the surface of~~ said layer of second material comprising steps of copper etch.

15. (currently amended) The method of claim 13, said step of removing said deposited layer of copper from ~~the surface of~~ said layer of second material comprising steps of Chemical Mechanical Polishing.

16. (original) The method of claim 1, said layer of IMD comprising a layer of low-k dielectric.

17. (original) The method of claim 1, said at least one opening having been created through said layer of IMD comprising applying a wet etch process.

18. (currently amended) A method of forming a dual damascene structure for copper dual damascene processes, comprising ~~the steps of~~:

providing a substrate, said substrate having been provided with semiconductor devices structures ~~in or on the surface thereof~~, at least one point of electrical contact having been provided in ~~the surface of~~ said substrate;

depositing a first layer of dielectric over ~~the surface of~~ said substrate;

creating at least one first opening through said first layer of dielectric, said at least one first opening being aligned with said at least one point of electrical contact ~~having been provided in the surface of said substrate~~;

creating a layer of protective material over a bottom surface of said at least one first opening;

baking said substrate, including said first layer of dielectric and said layer of protective material ~~over a bottom surface of said at least one first opening~~;

depositing a second layer of dielectric over ~~the surface of~~ said first layer of dielectric, filling said at least one first opening by depositing said second layer of dielectric over said layer of protective material;

creating at least one second opening through said second layer of dielectric, said at least one second opening being aligned with said at least one first opening, said at least one second opening comprising said at least one first opening where this at least one first opening extends above said layer of protective material.

19. (currently amended) The method of claim 18, said creating a layer of protective material over a bottom surface of said at least one first opening comprising ~~the steps of~~:

depositing a layer of protective material over ~~the surface of~~ said first layer of dielectric, filling said at least one opening created through said first layer of dielectric;

removing said layer of protective material from ~~the surface of~~ said first layer of dielectric, thereby partially removing said protective material from said at least one opening created through said first layer of dielectric, creating at least one partial opening through said first layer of dielectric, said at least one partial opening comprising:

(i) a layer of protective material over a bottom surface of said at least one first opening, and

(ii) a region overlying the layer of protective material from which said layer of protective material has been removed.

20. (original) The method of claim 19, said protective material comprising I-line photoresist.

21. (original) The method of claim 18, said first layer of dielectric comprising Inter Metal Dielectric (IMD).

22. (original) The method of claim 18, said second layer of dielectric comprising DUV photoresist.

23. (currently amended) The method of claim 18, said baking ~~said substrate, including said first layer of dielectric and said layer of protective material over a bottom surface of said at least one first opening~~ comprising baking said substrate for a period of time by applying an elevated temperature in a gaseous environment and under a pressure to said substrate.

24. (original) The method of claim 23, wherein said baking said substrate comprises baking said substrate on a hot plate.

25. (original) The method of claim 23, wherein said baking said substrate comprises baking said substrate inside a high-temperature furnace.

26. (original) The method of claim 23, wherein said applying an elevated temperature comprises applying a temperature between about 200 and 400 degrees C.

27. (original) The method of claim 23, wherein said pressure comprises a low pressure environment of between about 40 and 60 pa.

28. (original) The method of claim 23, wherein said pressure comprises an atmospheric pressure.

29. (original) The method of claim 23, wherein said gaseous environment may or may not contain an inert gas.

30. (original) The method of claim 23, wherein said gaseous environment may or may not contain an annealing agent that is typically applied for an anneal environment in which a metal is present.

31. (original) The method of claim 30, wherein said annealing agent is selected from the group consisting of H_2 and N_2 and NH_3.

32. (original) The method of claim 23, wherein said period of time is between about 1 and 30 minutes.

33. (currently amended) The method of claim 18, with additional steps being performed after creating at least one second opening

through said second layer of dielectric, said additional steps comprising:

depositing a layer of copper over ~~the surface of~~ said second layer of dielectric, thereby filling said at least one opening created through said second layer of dielectric that aligns with said at least one partial opening created through said first layer of dielectric, thereby further filling said at least one partial opening created through said first layer of dielectric; and

removing said deposited layer of copper from ~~the surface of~~ said second layer of dielectric.

34. (currently amended) The method of claim 33, said step of removing said deposited layer of copper from ~~the surface of~~ said second layer of dielectric comprising steps of copper etch.

35. (currently amended) The method of claim 33, said step of removing said deposited layer of copper from ~~the surface of~~ said second layer of dielectric comprising steps of Chemical Mechanical Polishing.

36. (original) The method of claim 18, said first layer of dielectric comprising a layer of low-k dielectric.

37. (original) The method of claim 18, said at least one opening having been created through said first layer of dielectric comprising applying a wet etch process.

Please enter the following new claims.

38. The method of claim 1, said at least one opening being created in preparation for creating a damascene or a dual damascene structure, said at least one opening comprising an I-line plug for devices having deep sub-micron dimensions.

39. The method of claim 1, said at least one partial opening being aligned with said at least one opening, said at least one partial opening comprising a first cross section comprising remnants of said first material remaining in place over a bottom surface of said at least one opening, said at least one partial opening further comprising a second cross section overlying said first cross section and from which said first material has been removed.

40. The method of claim 1, said baking comprising removing moisture from the layer of first material, thereby preventing

formation of scum deposits over the first cross of said at least one opening, thereby removing an inhibitor to removing a layer of second material from above the first cross section of said at least one opening since moisture is no longer present in the layer of first material during etching of the layer of second material.

41. The method of claim 1, said layer of second material having a cross-link lambda parameter that is different from the cross-link lambda parameter of the layer of first material, thereby allowing selective exposures of the layers of first and second material.

42. The method of claim 18, said at least one opening being created in preparation for creating a damascene or a dual damascene structure, said at least one opening comprising an I-line plug for devices having deep sub-micron dimensions.

43. The method of claim 18, said baking comprising removing moisture from the first layer of dielectric, thereby preventing formation of scum deposits over the layer of protective material, thereby removing an inhibitor to removing a second layer of dielectric from above the layer of protective material

since moisture is no longer present in the first layer of dielectric during etching of the second layer of dielectric.

44 The method of claim 18, said second layer of dielectric having a cross-link lambda parameter that is different from the cross-link lambda parameter of the first layer of dielectric, thereby allowing selective exposures of the first and second layers of dielectric.